FIG. 1

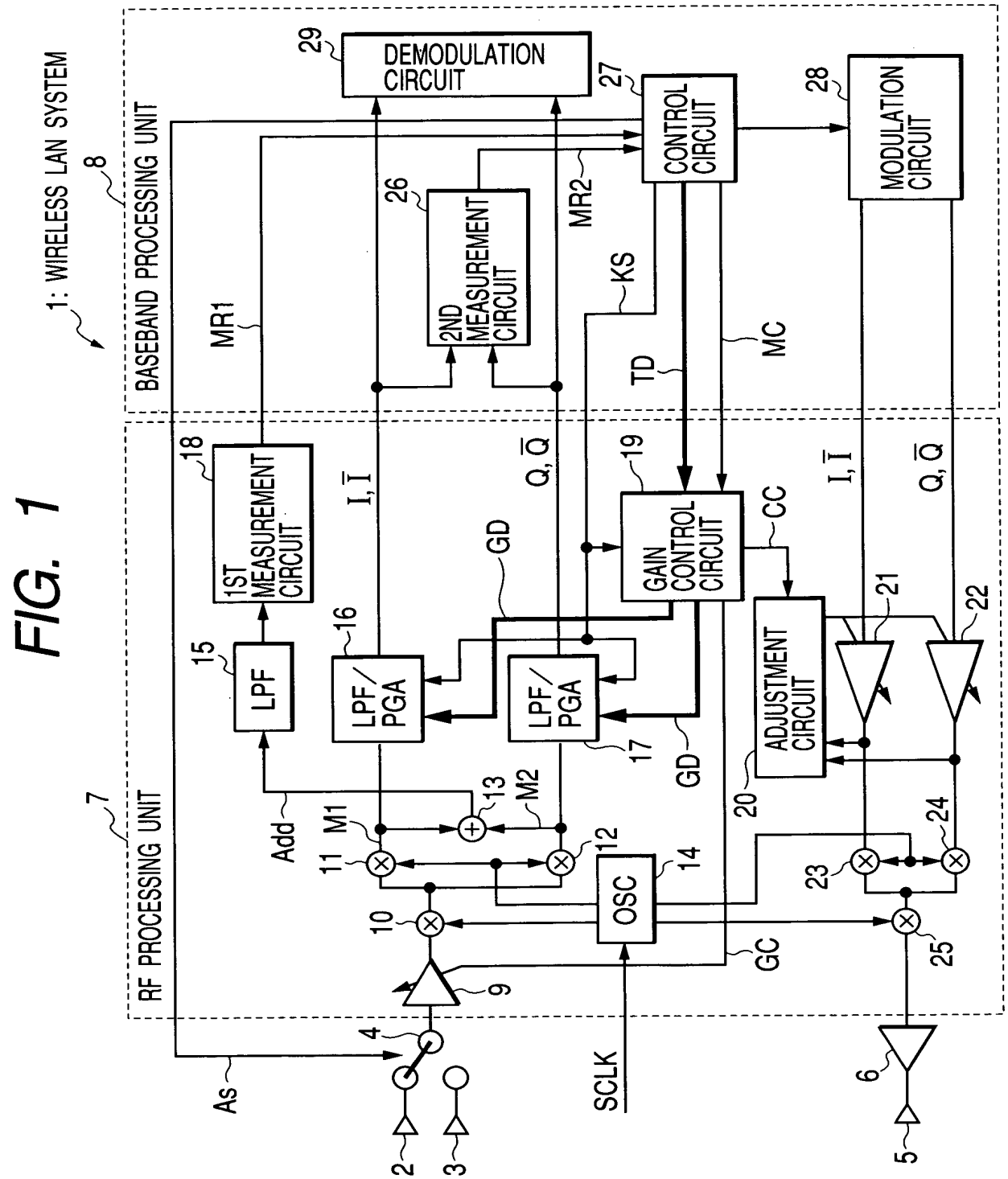

1: WIRELESS LAN SYSTEM
BASEBAND PROCESSING UNIT
RF PROCESSING UNIT
DEMODULATION CIRCUIT
CONTROL CIRCUIT
MODULATION CIRCUIT
2ND MEASUREMENT CIRCUIT
1ST MEASUREMENT CIRCUIT
GAIN CONTROL CIRCUIT
ADJUSTMENT CIRCUIT
LPF
LPF/PGA
LPF/PGA
OSC
MR1
MR2
KS
TD
MC
GD
CC
GC
I, Ī
Q, Q̄
Add
M1
M2
As
SCLK

FIG. 2

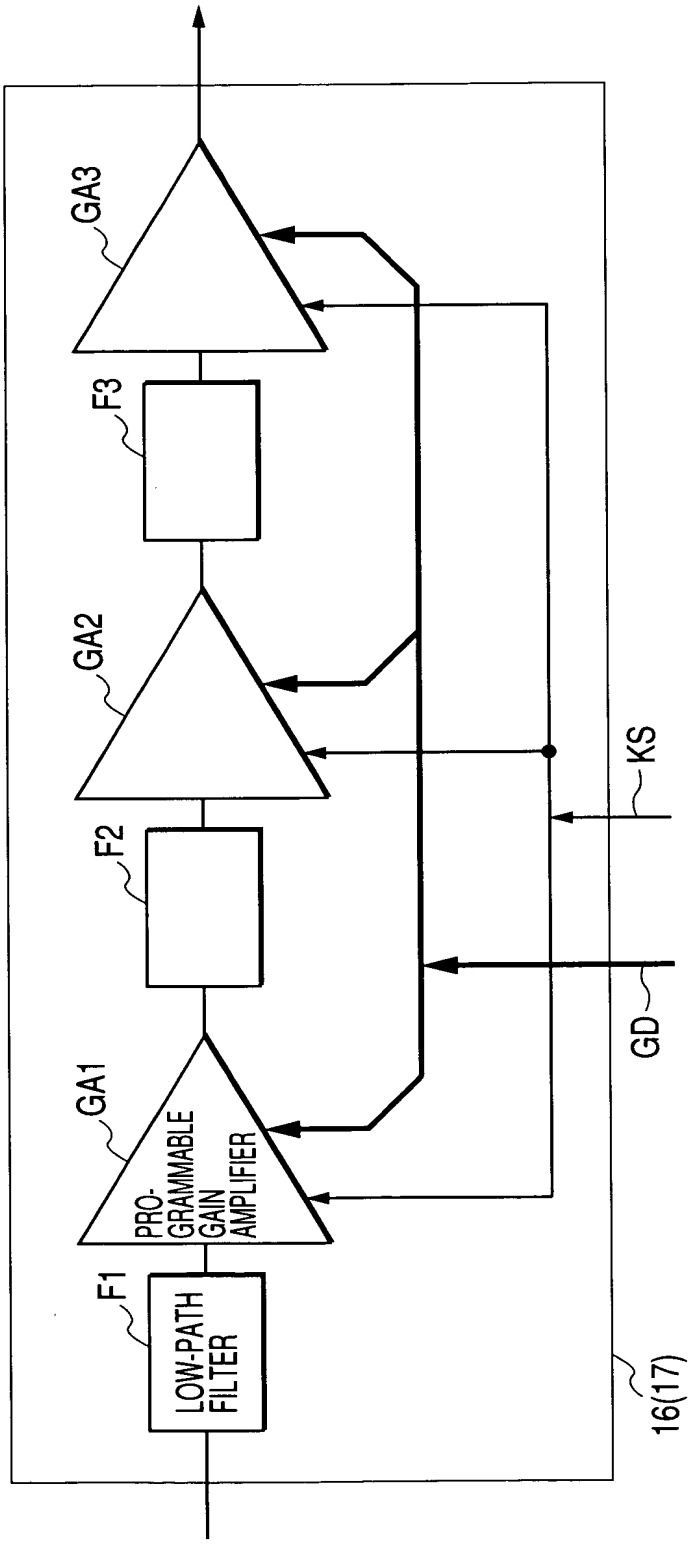

GA3
F3
GA2
F2
GA1
PRO-
GRAMMABLE
GAIN
AMPLIFIER
F1
LOW-PATH
FILTER
KS
GD
16(17)

FIG. 3

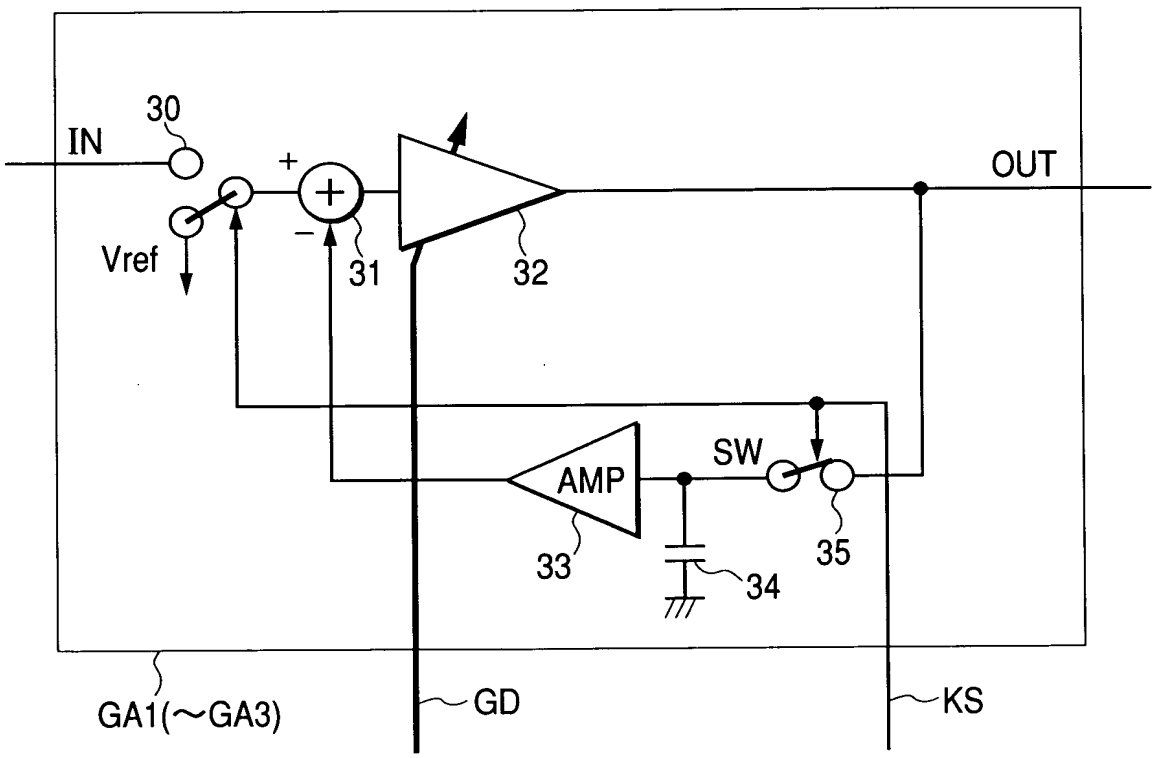


FIG. 4

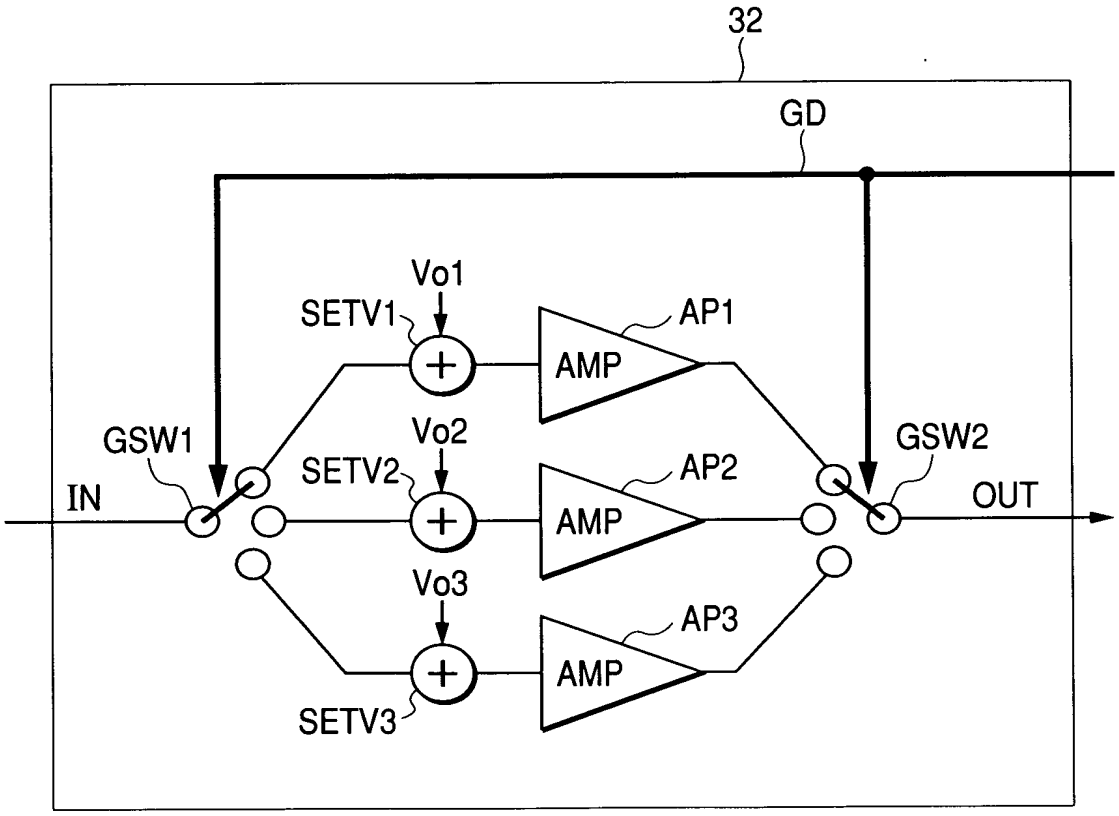

32
GD
Vo1
SETV1
AP1
AMP
GSW1
Vo2
SETV2
AP2
AMP
GSW2
IN
OUT
Vo3
AP3
AMP
SETV3

FIG. 5

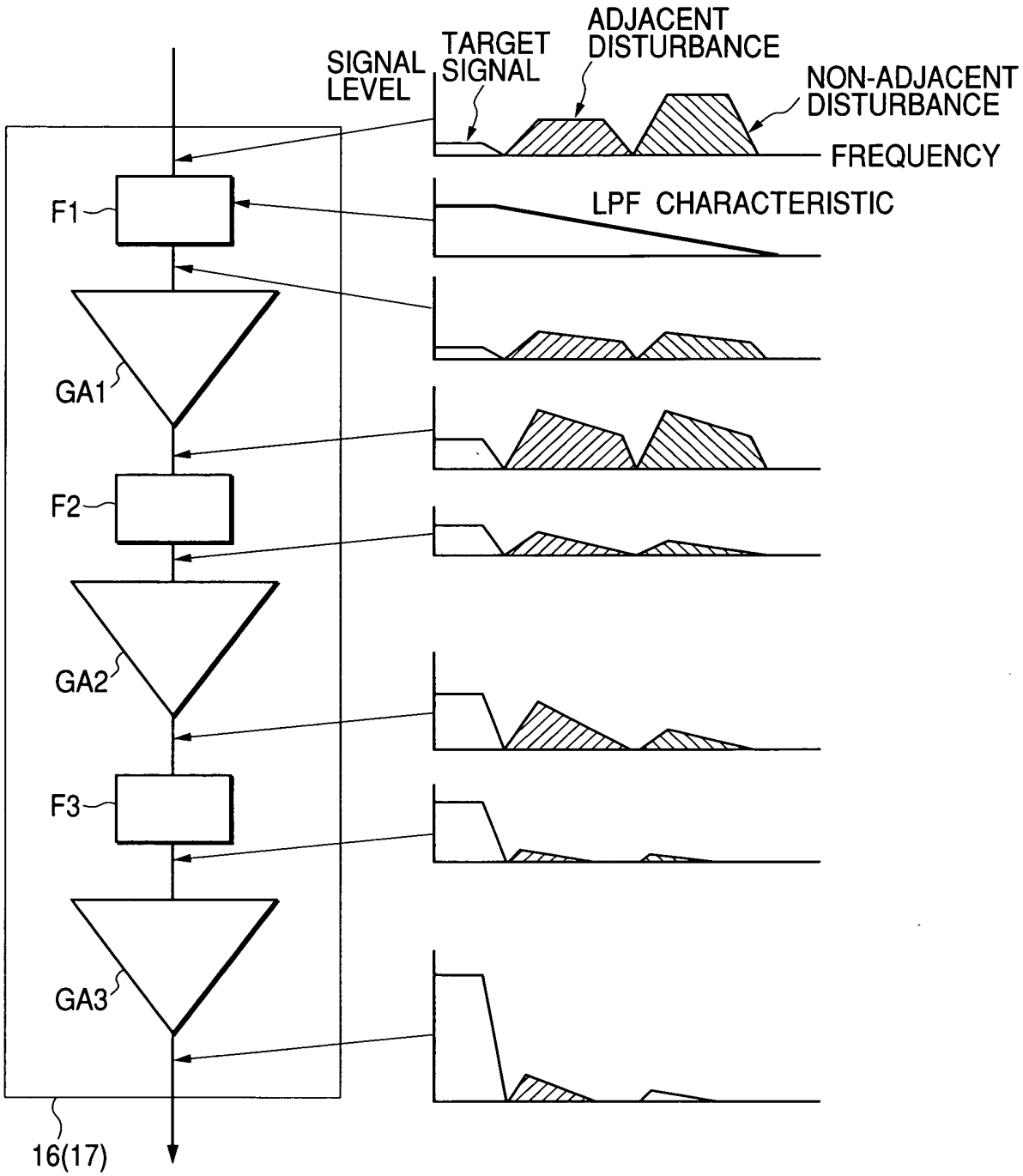

SIGNAL LEVEL
TARGET SIGNAL
ADJACENT DISTURBANCE
NON-ADJACENT DISTURBANCE
FREQUENCY
LPF CHARACTERISTIC
F1
GA1
F2
GA2
F3
GA3
16(17)

FIG. 6

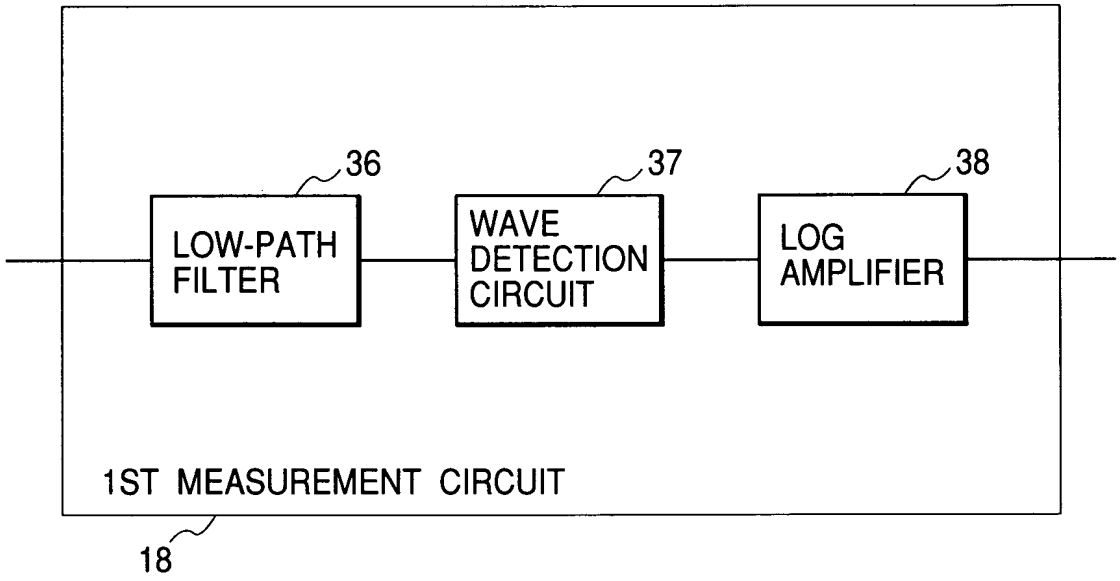

36
37
38
LOW-PATH FILTER
WAVE DETECTION CIRCUIT
LOG AMPLIFIER
1ST MEASUREMENT CIRCUIT
18

FIG. 7

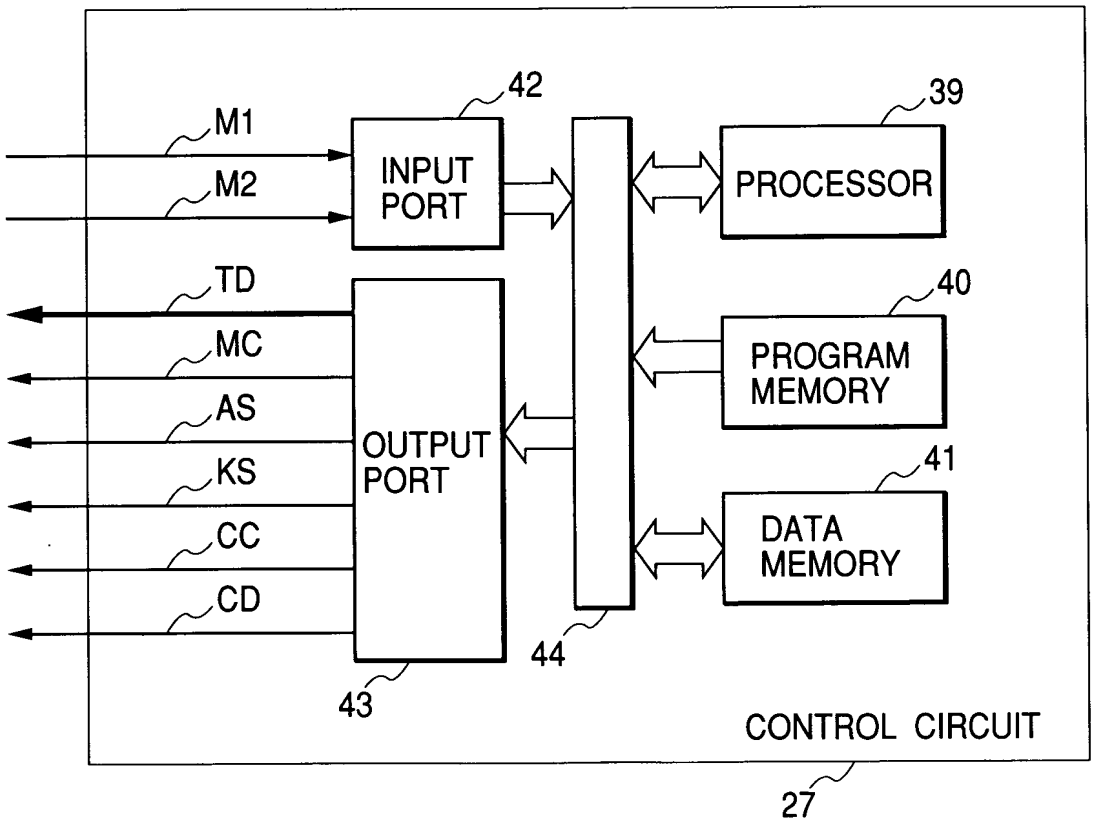

M1
M2
TD
MC
AS
KS
CC
CD
INPUT PORT
OUTPUT PORT
42
43
44
39
PROCESSOR
40
PROGRAM MEMORY
41
DATA MEMORY
CONTROL CIRCUIT
27

FIG. 8

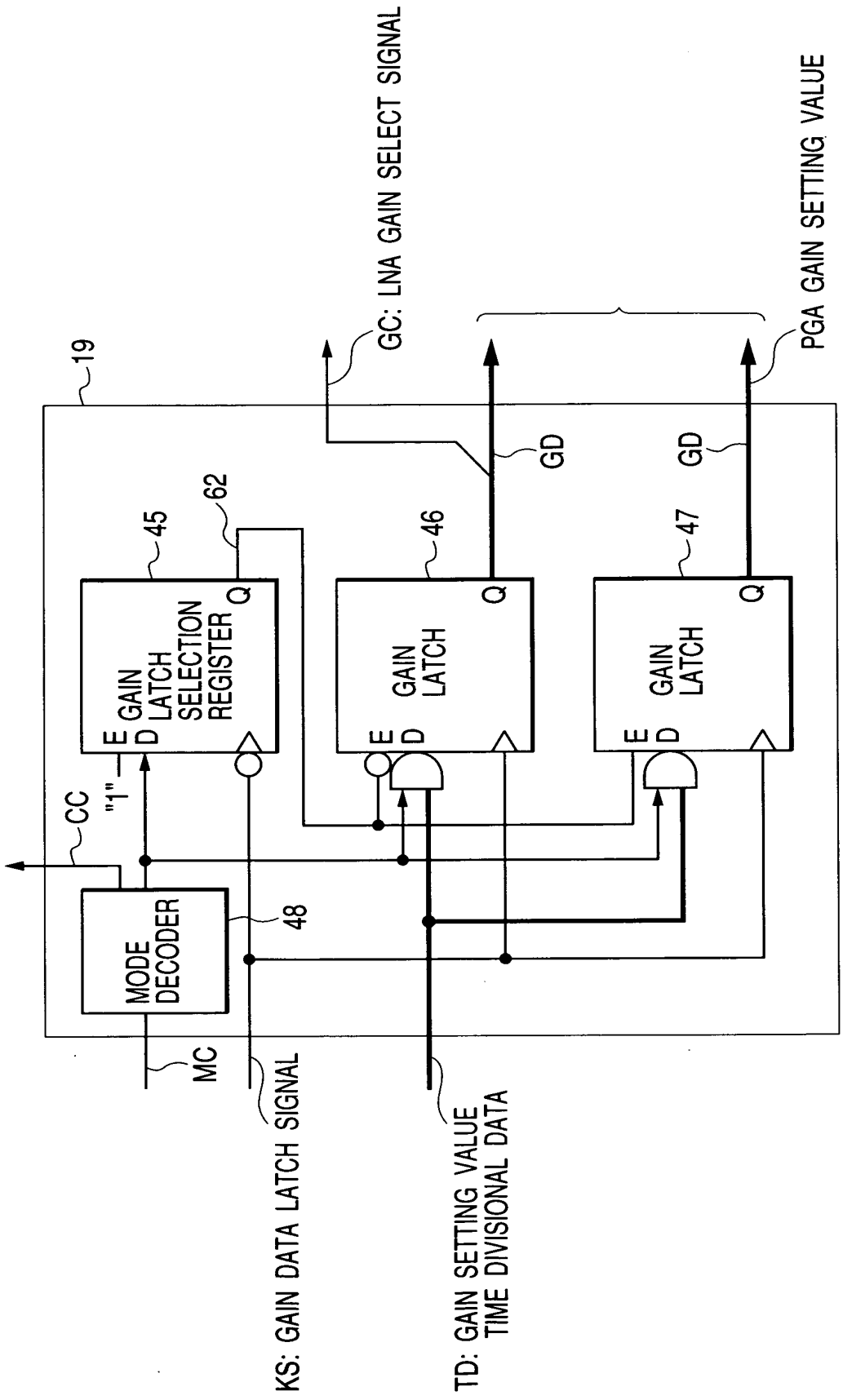

19
GC: LNA GAIN SELECT SIGNAL
PGA GAIN SETTING VALUE
GD
GD
45
62
46
47
GAIN LATCH SELECTION REGISTER
GAIN LATCH
GAIN LATCH
E
D
Q
CC
"1"
MODE DECODER
48
MC
KS: GAIN DATA LATCH SIGNAL
TD: GAIN SETTING VALUE TIME DIVISIONAL DATA

FIG. 9

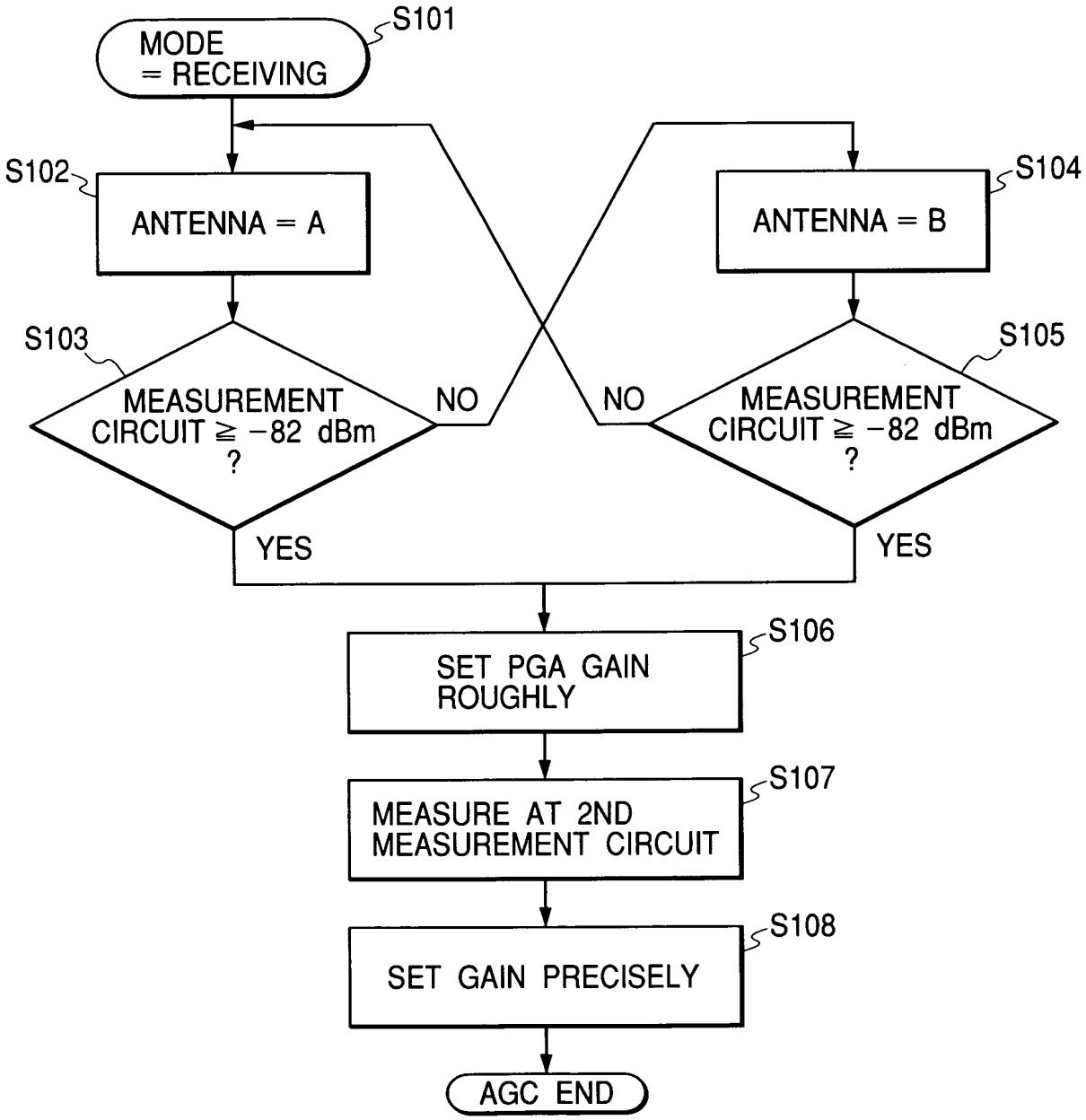

MODE
= RECEIVING
S101
S102
ANTENNA = A
S103
MEASUREMENT
CIRCUIT ≧ −82 dBm
?
NO
YES
S104
ANTENNA = B
S105
MEASUREMENT
CIRCUIT ≧ −82 dBm
?
NO
YES
S106
SET PGA GAIN
ROUGHLY
S107
MEASURE AT 2ND
MEASUREMENT CIRCUIT
S108
SET GAIN PRECISELY
AGC END

FIG. 10

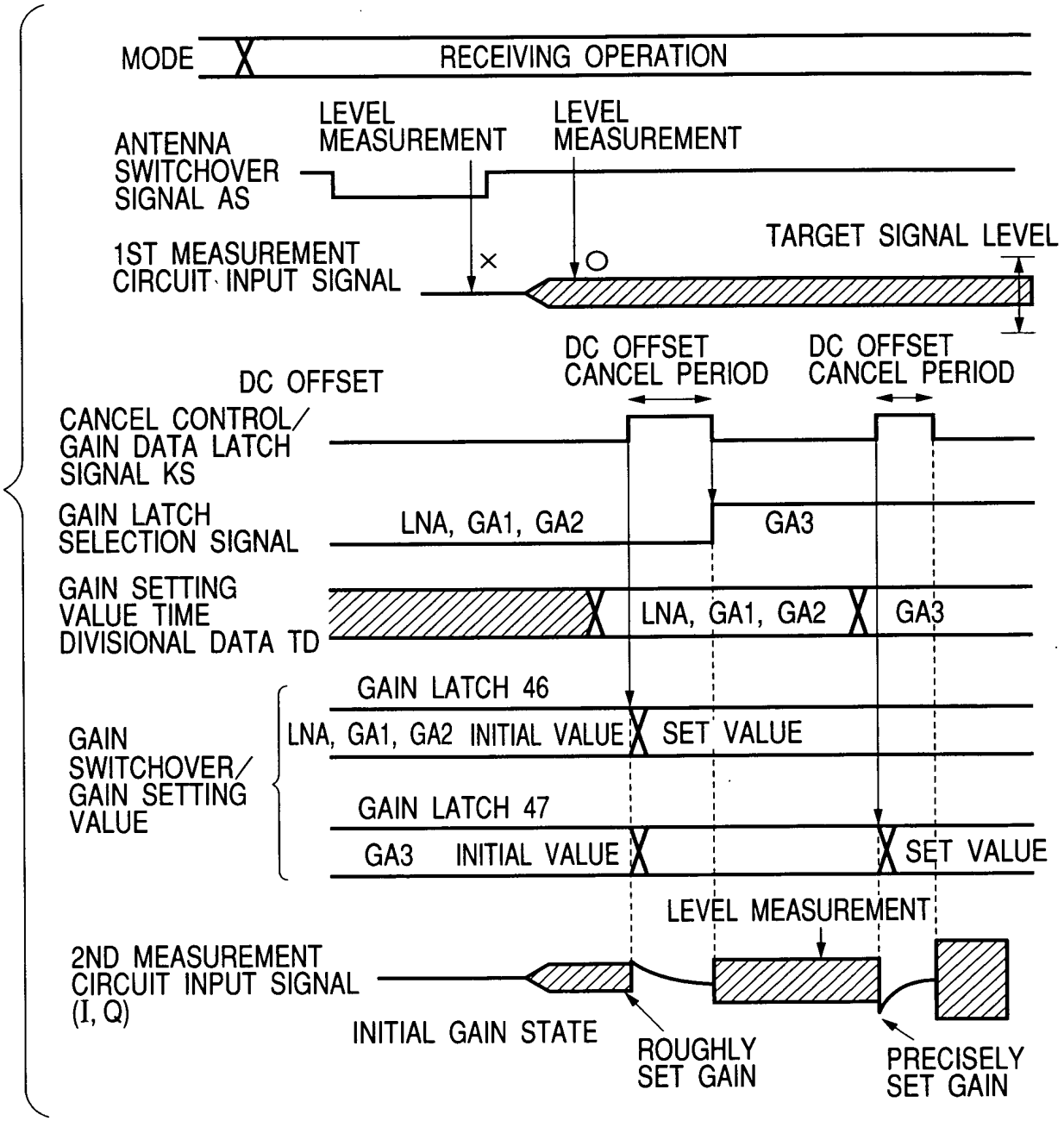

MODE
RECEIVING OPERATION
LEVEL MEASUREMENT
LEVEL MEASUREMENT
ANTENNA SWITCHOVER SIGNAL AS
1ST MEASUREMENT CIRCUIT INPUT SIGNAL
×
○
TARGET SIGNAL LEVEL
DC OFFSET
DC OFFSET CANCEL PERIOD
DC OFFSET CANCEL PERIOD
CANCEL CONTROL/ GAIN DATA LATCH SIGNAL KS
GAIN LATCH SELECTION SIGNAL
LNA, GA1, GA2
GA3
GAIN SETTING VALUE TIME DIVISIONAL DATA TD
LNA, GA1, GA2
GA3
GAIN SWITCHOVER/ GAIN SETTING VALUE
GAIN LATCH 46
LNA, GA1, GA2 INITIAL VALUE
SET VALUE
GAIN LATCH 47
GA3 INITIAL VALUE
SET VALUE
LEVEL MEASUREMENT
2ND MEASUREMENT CIRCUIT INPUT SIGNAL (I, Q)
INITIAL GAIN STATE
ROUGHLY SET GAIN
PRECISELY SET GAIN

FIG. 11

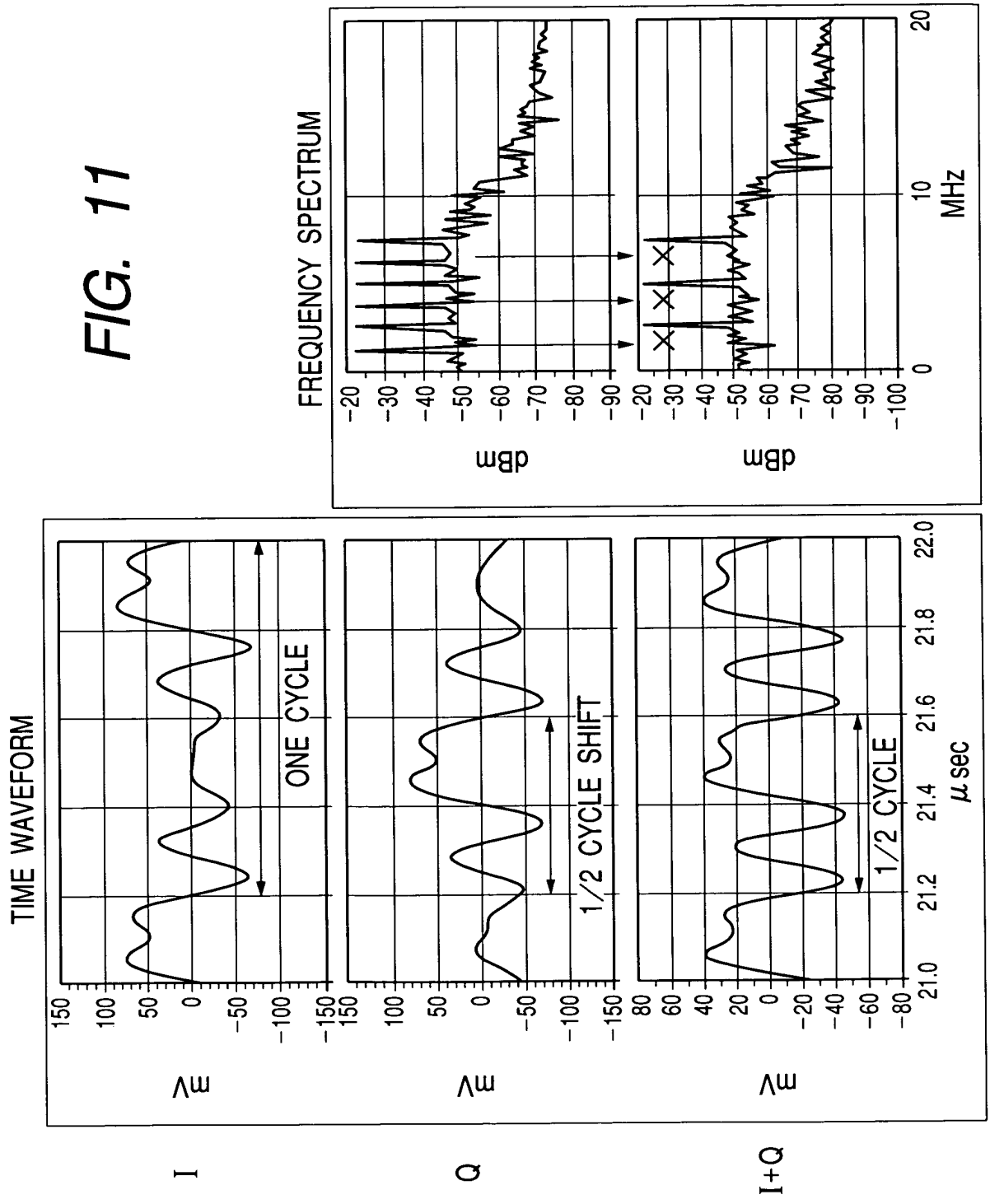

TIME WAVEFORM
FREQUENCY SPECTRUM
I
Q
I+Q
mV
dBm
ONE CYCLE
1/2 CYCLE SHIFT
1/2 CYCLE
μsec
MHz

FIG. 12

TERMINAL NAME		ATTRIBUTE	FUNCTION	REMARK	CORRESPONDENCE TO SYMBOLS IN FIG. 1
RECEIVED SIGNAL	RSSIOUT	OUT/Analog	RSSI OUTPUT		MEASURED SIGNAL MRI
	RXBBOUTIX	OUT/Analog	RECEIVED BASEBAND I SIGNAL (Positive)		I SIGNAL
	RXBBOUTIY	OUT/Analog	RECEIVED BASEBAND I SIGNAL (Negative)		
	RXBBOUTQX	OUT/Analog	RECEIVED BASEBAND Q SIGNAL (Positive)		Q SIGNAL
	RXBBOUTQY	OUT/Analog	RECEIVED BASEBAND Q SIGNAL (Negative)		
CONTROL SIGNAL	AGCGAIN [3]	IN/Digital	AGC GAIN SETTING VALUE INPUT, MSB	(SEE FIG. 11)	GAIN SETTING VALUE TIME DIVISION DATA TD
	AGCGAIN [2]	IN/Digital	AGC GAIN SETTING VALUE INPUT		
	AGCGAIN [1]	IN/Digital	AGC GAIN SETTING VALUE INPUT		
	AGCGAIN [0]	IN/Digital	AGC GAIN SETTING VALUE INPUT, LSB		
	WAIT	IN/Digital	AGC GAIN SETTING VALUE LATCHING TIMING & DC OFFSET SETTING CONTROL		DC OFFSET CANCEL CONTROL/GAIN DATA LATCH SIGNAL KS
	MODE [2]	IN/Digital	INPUT FOR OPERATION AND POWER SAVING MODE SETTING	(SEE TABLE 2-(1))	MODE CONTROL SIGNAL MC
	MODE [1]	IN/Digital			
	MODE [0]	IN/Digital			
	LE	IN/Digital	3-wire interface, LOAD ENABLE	(SEE TABLE 2-(2)) (SEE FIG. 15)	
	SDATA	IN/Digital	3-wire interface, SERIAL DATA		
	SCLK	IN/Digital	3-wire interface, SERIAL CLOCK		
	REFCLK	IN/Digital	20MHz REFERENCE CLOCK INPUT		REFERENCE CLOCK SCLK
SIGNAL TO SEND	TXBBINIX	IN/Analog	BASEBAND I SIGNAL TO SEND (Positive)		I SIGNAL
	TXBBINIY	IN/Analog	BASEBAND I SIGNAL TO SEND (Negative)		
	TXBBINQX	IN/Analog	BASEBAND Q SIGNAL TO SEND (Positive)		Q SIGNAL
	TXBBINQY	IN/Analog	BASEBAND Q SIGNAL TO SEND (Negative)		

FIG. 13

Bit			Description		
MODE [2]	MODE [1]	MODE [0]	Mode	Status	Power-on Block
0	0	0	Idle	MAXIMUM POWER SAVING	—
0	0	1	Pre-Heat	ONLY BGR CIRCUIT ON	
0	1	0	Warm-Up	BGR-Synthesizer OPERATION	
0	1	1	TX-Cal	TRANSMISSION BLOCK CALIBRATION	
0	0	0	RX-Cal	RECEIVING BLOCK CALIBRATION	
1	0	1	RX	RECEIVING OPERATION	
1	1	0	TX	TRANSMISSION OPERATION	
1	1	1	TBD	TBD	TBD

FIG. 14

Register	Word #	Serial Bits						
	LSB	2	3	4	5	6	7	8	MSB
Test	0	0	T0	T1	T2	T3	T4	T5	T6
Synth Ch	0	1	SR	C0	C1	C2	C3	C4	C5
TX Power	1	0	P0	P1	P2	P3	Don't Care		
(TBD)	1	1	(TBD)						

FIG. 15

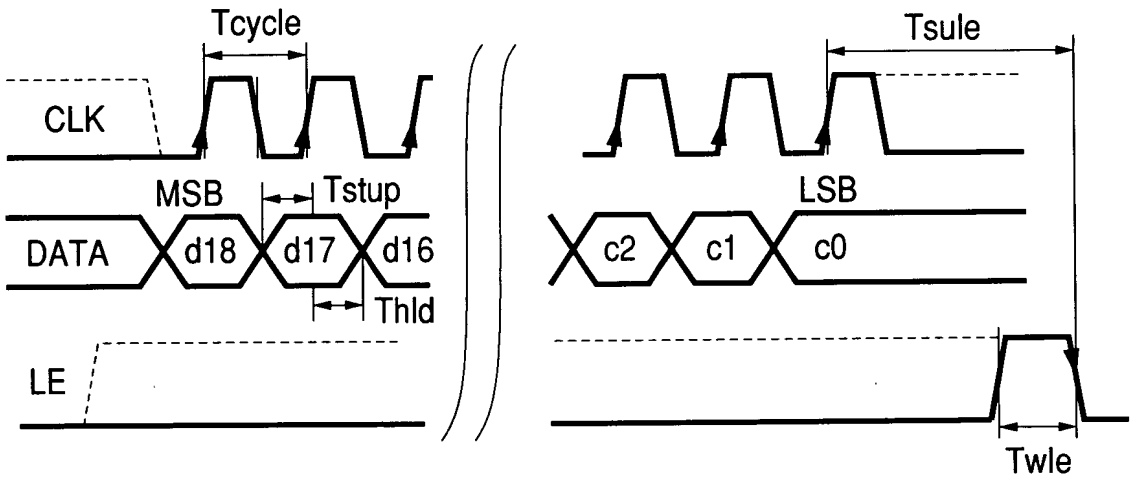

Tcycle
Tsule
CLK
MSB
Tstup
LSB
DATA
d18
d17
d16
c2
c1
c0
Thld
LE
Twle

FIG. 16

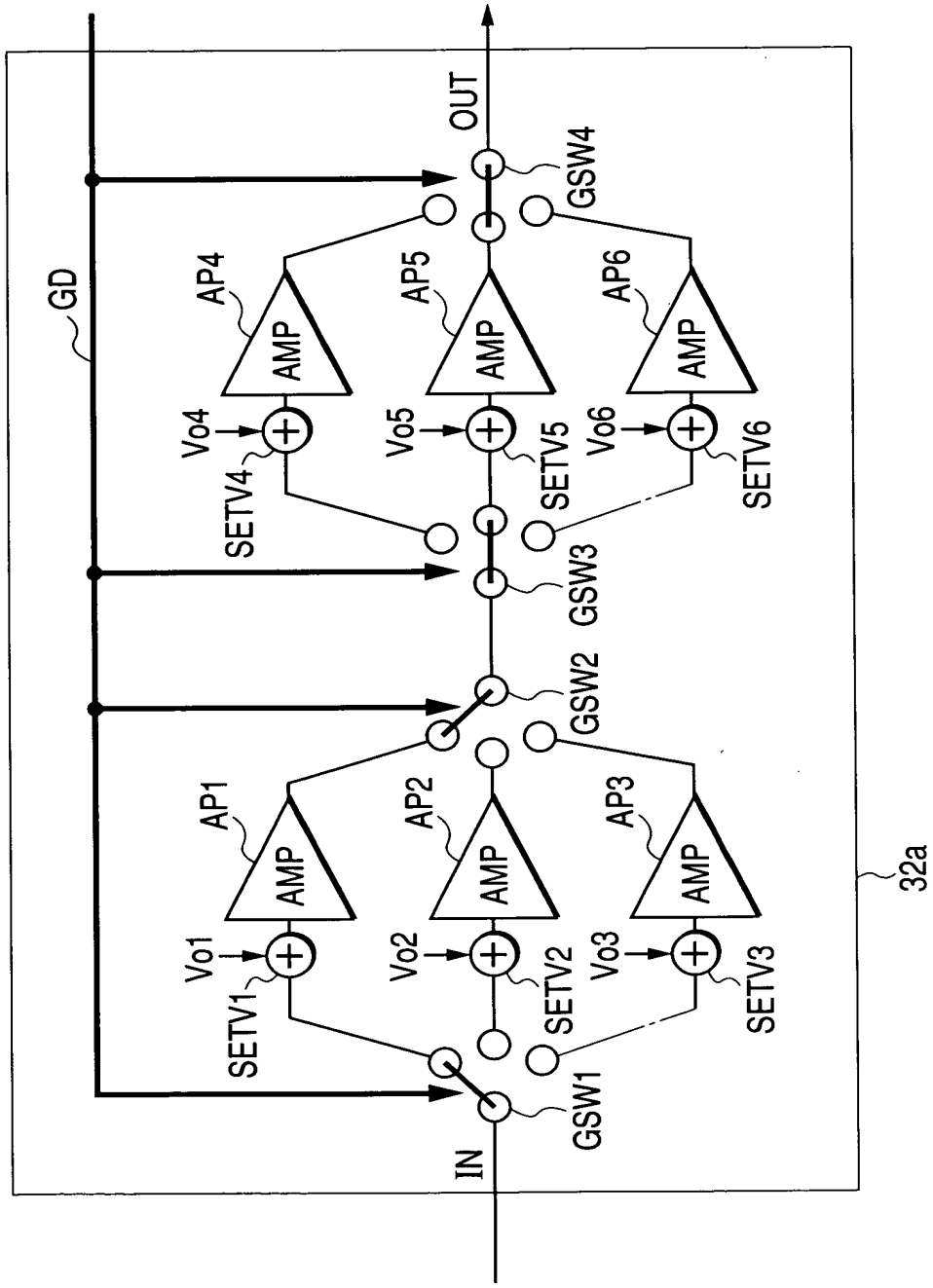

GD
OUT
IN
GSW1
GSW2
GSW3
GSW4
AP1
AP2
AP3
AP4
AP5
AP6
AMP
Vo1
Vo2
Vo3
Vo4
Vo5
Vo6
SETV1
SETV2
SETV3
SETV4
SETV5
SETV6
32a

FIG. 17

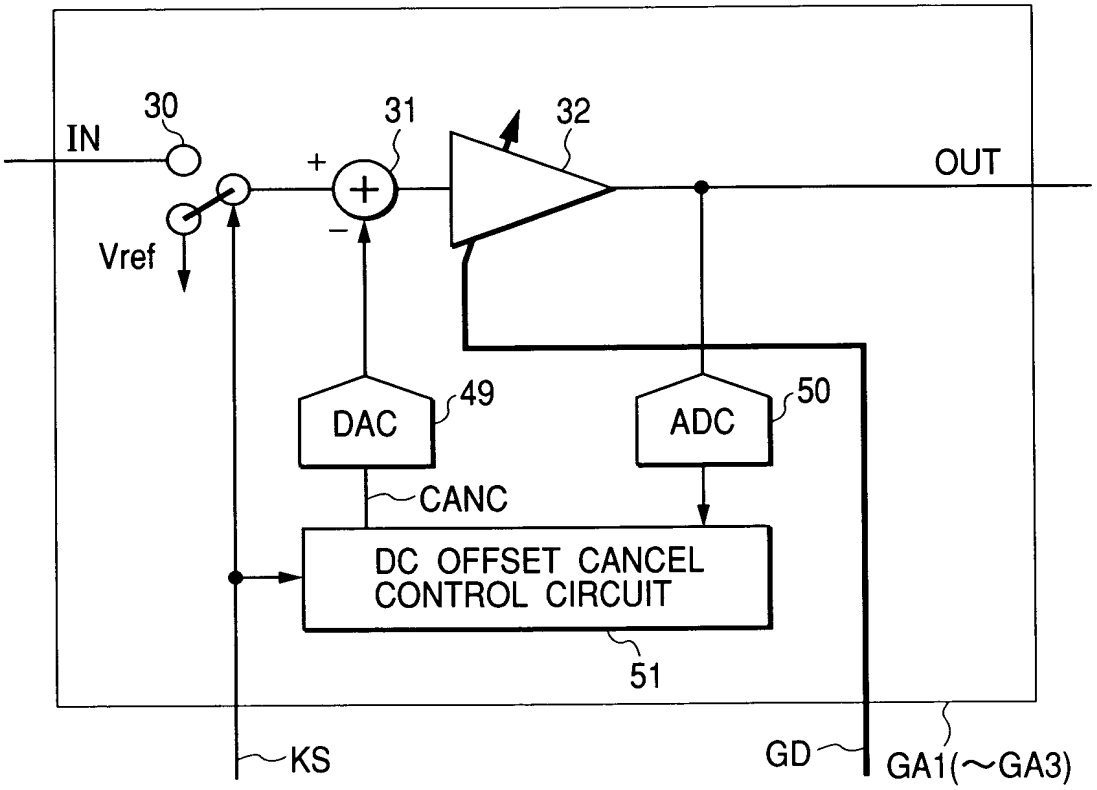

IN
30
31
32
OUT
+
−
Vref
DAC
49
ADC
50
CANC
DC OFFSET CANCEL
CONTROL CIRCUIT
51
KS
GD
GA1(~GA3)

FIG. 18

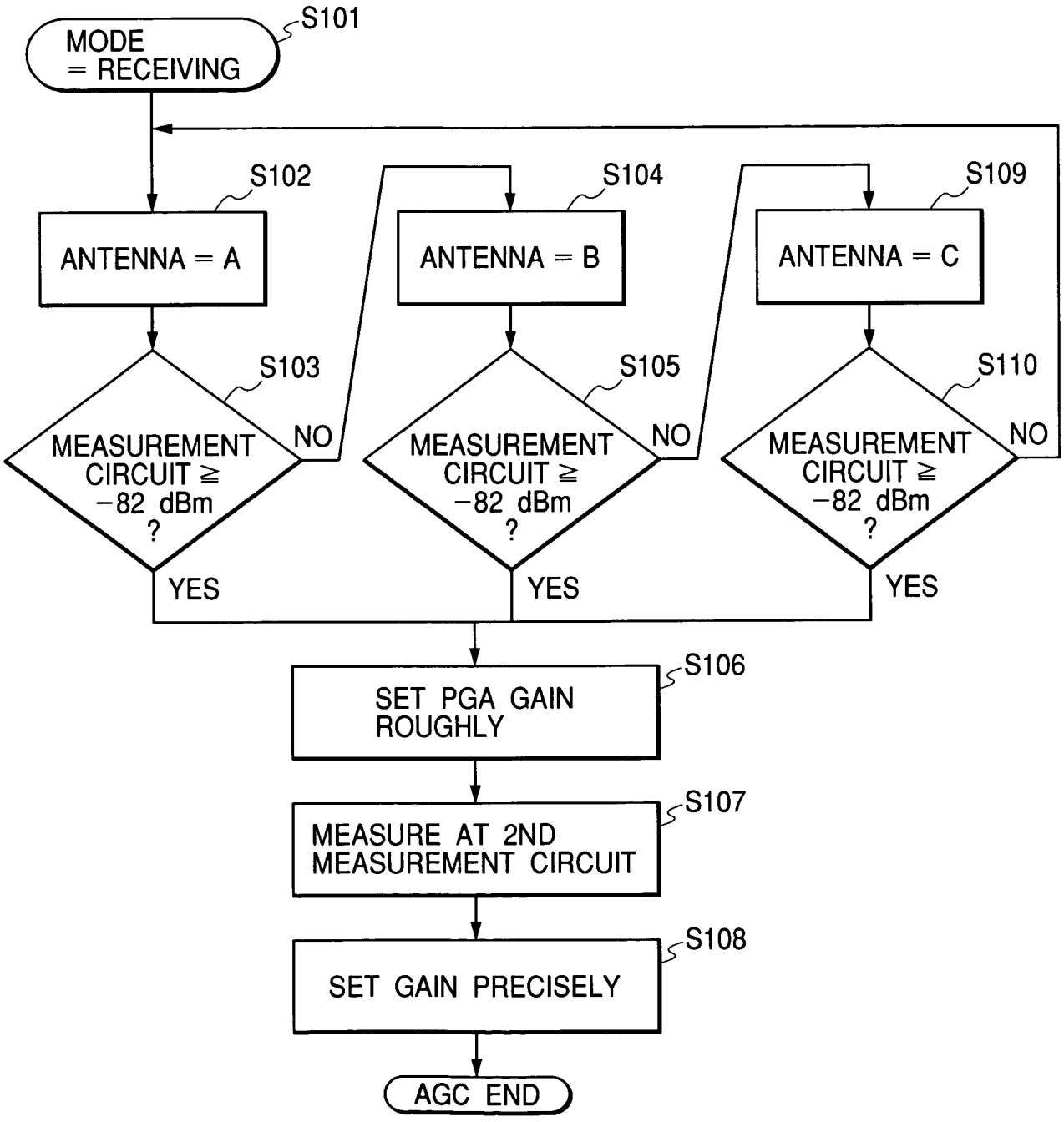

MODE
= RECEIVING
S101
S102
ANTENNA = A
S103
MEASUREMENT CIRCUIT ≧ −82 dBm ?
NO
YES
S104
ANTENNA = B
S105
MEASUREMENT CIRCUIT ≧ −82 dBm ?
NO
YES
S109
ANTENNA = C
S110
MEASUREMENT CIRCUIT ≧ −82 dBm ?
NO
YES
S106
SET PGA GAIN ROUGHLY
S107
MEASURE AT 2ND MEASUREMENT CIRCUIT
S108
SET GAIN PRECISELY
AGC END

FIG. 19

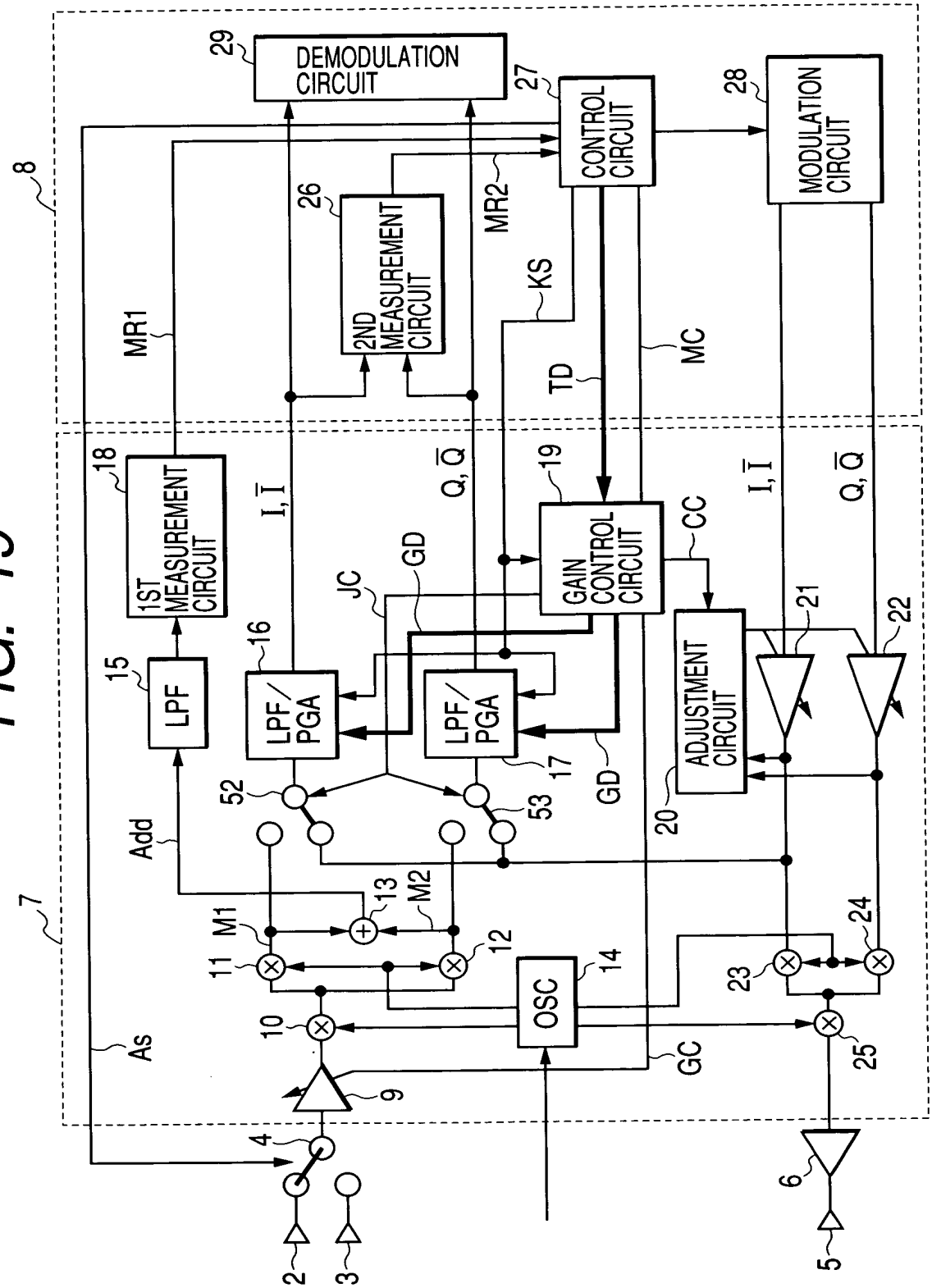
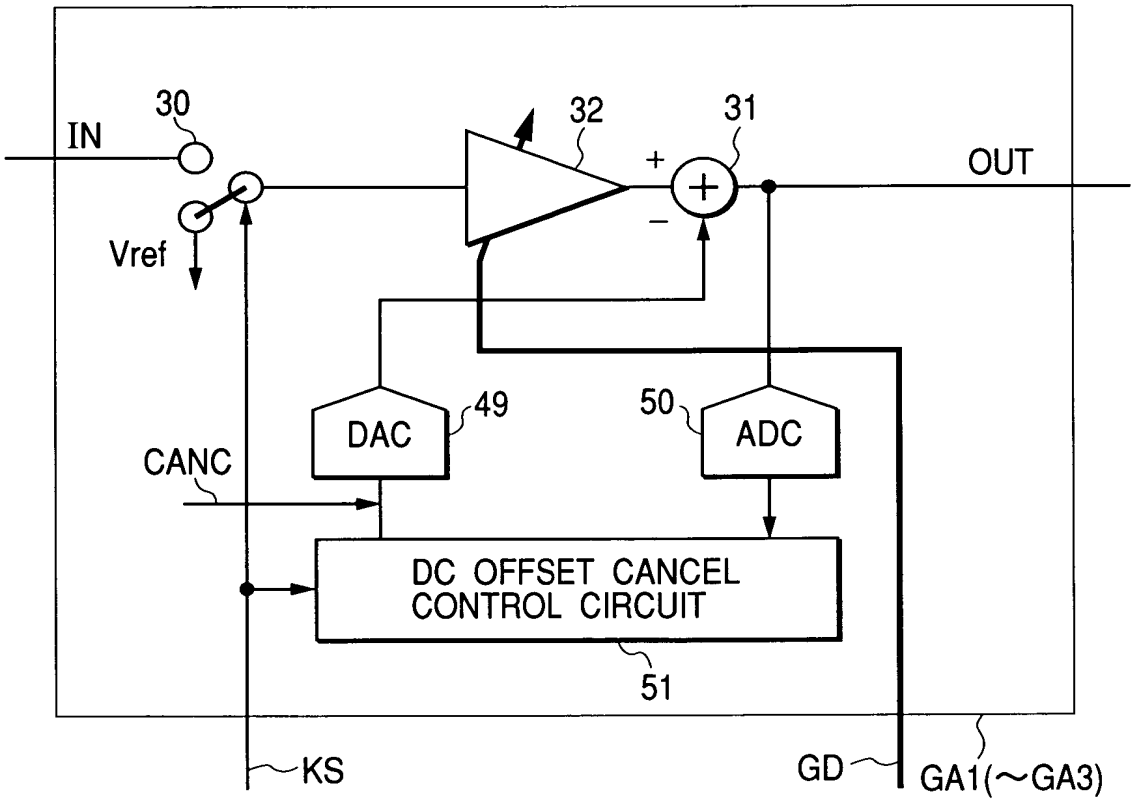

8
7
29
DEMODULATION CIRCUIT
27
CONTROL CIRCUIT
28
MODULATION CIRCUIT
26
2ND MEASUREMENT CIRCUIT
MR1
MR2
KS
TD
MC
18
1ST MEASUREMENT CIRCUIT
I, Ī
Q, Q̄
19
GAIN CONTROL CIRCUIT
CC
JC
GD
15
LPF
16
LPF/PGA
17
LPF/PGA
52
53
Add
M1
M2
13
11
12
OSC
14
10
As
9
4
2
3
20
ADJUSTMENT CIRCUIT
21
22
23
24
25
6
5
GC

FIG. 20


IN
30
32
31
+
OUT
Vref
−
DAC
49
50
ADC
CANC
DC OFFSET CANCEL
CONTROL CIRCUIT
51
KS
GD
GA1(~GA3)